REMARKS

Applicants gratefully acknowledge the Examiner's statement that claims 1-4, 6-13, 16-21, 24, 28-32, 35, 37-41 and 44-48 contain allowable subject matter. Claims 49 and 50 have been canceled without prejudice. Claims 51 and 52 have been newly added. Claims 1-4, 6-13, 16-21, 24, 27-32, 35-41, 44-48, 51 and 52 are now pending in this case.

Applicants are filing a Supplemental Information Disclosure Statement concurrently with this amendment and respectfully request that the Examiner consider the references disclosed therein.

Claims 27 and 36 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Buerger, Jr. (U.S. Patent Application Publication No. US 2002/0050606 A1). Applicants respectfully traverse the rejection and request reconsideration.

Claims 27 and 36 recite a semiconductor memory structure comprising "a programmable conductor memory element, a first terminal of which is coupled to [a] column line and a second terminal of which is coupled to a first side of a reverse connected diode pair." [Emphasis added]. A programmable conductor memory element is one in which stable low and high resistance states can be used to store binary data. Buerger does not teach or suggest a programmable conductor memory element, much less to include a programmable conductor memory element in a semiconductor memory structure as defined by claim 27 and 36.

To the contrary, Buerger merely discloses a floating cell memory array made of memory cells using capacitors and diodes. At least for this reason, claims 27 and 36 are not anticipated by Buerger and the rejection of claims 27 and 36 should be withdrawn.

Claims 28-32, 35, 37-41 and 44 depend from claims 27 and 36. Accordingly, claims 28-32, 35, 37-41 and 44 are allowable over Buerger at least for the reasons described above in connection with claims 27 and 36, and also because Buerger fails to

teach or suggest the respective inventive combinations defined by claims 28-32, 35, 37-41 and 44.

Claims 49 and 50 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Harshfield (U.S. Patent No. 5,818,749). Claims 49 and 50 have been canceled without prejudice, and therefore, this rejection is no longer applicable.

Newly added claim 51 recites a method of sensing a stored value of a variable resistance random access memory element, comprising "discharging [a] voltage level . . . through said memory element and also through a reverse connected diode pair in series with said memory element . . . to determine a logical state of said memory element. [Emphasis added]. None of the cited references, taken alone or in combination, teach or suggest the inventive combination defined by claim 51.

Newly added claim 52 recites a semiconductor memory structure, comprising "a variable resistive memory element, a first terminal of which is coupled to [a] column line and a second terminal of which is coupled to a first side of a reverse connected diode pair." [Emphasis added]. None of the cited references, taken alone or in combination, teach or suggest the inventive combination defined by claim 52.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application (with claims 1-4, 6-13, 16-21, 24, 27-32, 35-41, 44-48, 51 and 52) to issue.

Dated: August 15, 2003

Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No. 28,371
Salvatore P. Tamburo
Registration No. 45,153
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700

Attorneys for Applicants